ALevel CS C18 Hardware and virtual machine

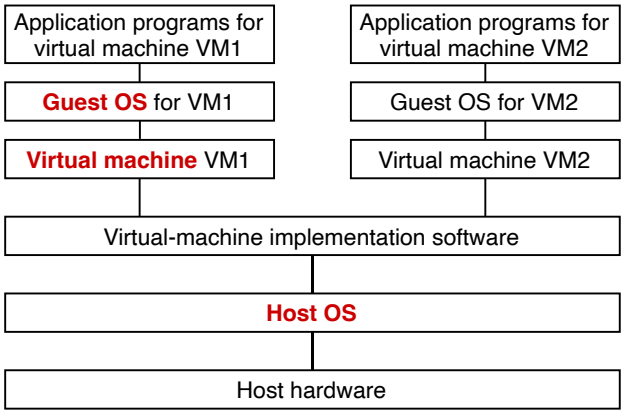
Control Unit

Control Unit: to ensure that each machine instruction is handled correctly
Two methods control unit can be designed:
1. **logic circuit**: hardware solution. The machine-code instructions are handled directly by hardware.
2. **microprogramming**: contains a ROM component that stores the microinstructions or microcode for microprogramming, often referred to as firmware.

CISC and RISC processor

Complex Instruction Set Computer (CISC): a single instruction can be more complex and involve more loading of data from memory
Reduced Instruction Set Computer (RISC): a single instruction is simpler, requiring minimal loading of data from memory
CISC and RISC point:
1. For RISC the term 'reduced' affects more than just the number of instructions.
2. A reduction in the number of instructions is not the major driving force for the use of RISC.
3. The reduction in the complexity of the instructions is a key feature of RISC.
4. The typical CISC architecture contains many specialised instructions.
5. The specialised instructions are designed to match the requirement of a high-level programming language.
6. The specialised instructions require multiple memory accesses which are very slow compared with register accesses.
7. The simplicity of the instructions for a RISC processor allows data to be stored in registers and manipulated in them with no resource to memory access other than that necessary for initial loading and possible final storing.
8. The simplicity of RISC instructions makes it easier to use hard-wiring inside the control unit.
9. The complexity of many of the CISC instructions makes hard-wiring much more difficult so microprogramming is the norm.

RISC	CISC
Fewer instructions	More instructions
Simpler instructions	More complex instructions
Small number of instruction formats	Many instruction formats
Single-cycle instructions whenever possible	Multi-cycle instructions
Fixed-length instructions	Variable-length instructions
Only load and store instructions to address memory	Many types of instructions to address memory
Fewer addressing modes	More addressing modes
Multiple register sets	Fewer registers
Hard-wired control unit	Microprogrammed control unit
Pipelining easier	Pipelining more difficult



Pipelining

Pipelining: instruction-level parallelism. a technique used to **improve the execution throughput of a CPU** by using the processor resources in a more efficient manner

Colck cycle							
	1	2	3	4	5	6	7
Instruction fetch (IF)	1.1	2.1	3.1	4.1	5.1	6.1	7.1
Instruction decode(ID)		1.2	2.2	3.2	4.2	5.2	6.2
Operand fetch(OF)			1.3	2.3	3.3	4.3	4.3
Instruction execute(IE)				1.4	2.4	3.4	4.4
Result write back(WB)					1.5	2.5	3.5

Pipelining for five-stage instruction handling:
1. For pipelining to be implemented, the construction of the processor must have **five independent units**, with each handling one of the five stages identified.
2. Once under way, the pipeline is handling five stages of five individual instructions.
3. One issue with a pipelined processor is **interrupt handling**.
   1. erase the pipeline contents for the latest four instructions to have entered.
   2. construct the individual units in the processor with individual program counter registers.

Two issue will cause the pipeline to stall:
1. dealing with a **data dependency between instructions**
2. **branch instructions**

CISC and RISC processor

Parallel processing: means that the architecture has more than one processor. Different processors are responsible for different parts of tasks.
SISD: Single Instruction Stream Single Data stream; a single processor accessing one memory
SIMD: Single Instruction Stream Multiple Data stream; processing of parallel data input requiring one control unit instructing multiple processing units
MISD: Multiple Instruction Stream Single Data stream; does not exist in a single architecture
MIMD: Multiple Instruction Stream Multiple Data stream; multiple processors asynchronously processing parallel data input
Massively parallel computer systems:
1. a network infrastructure to support multiple computer units.
2. The programs running on the different computers can communicate by passing messages using the network
3. cluster computing using PCs
4. an extremely large number of individual processors working in parallel.

These are the systems used by large organisations for computations involving highly complex mathematical processing
Issue:
1. Communication between the different processors is the issue
2. Each processor needs a link to every other processor
3. Many processors require many of these links
4. Challenging topology

Virtual Machine

System virtual machine: the emulation of computer system hardware using software.
Virtual machine advantage:
1. more than one different operating system can be made available on one computer system
2. an organisation has legacy systems and wishes to continue to use the old software but does not wish to keep the old hardware.
3. the same operating system can be made available many times by companies with large mainframe computers that offer server consolidation facilities.

Virtual machine disadvantage:
1, the time and effort required for implementation
2. low performance